LAURENCE W. NAGEL
Omega Enterprises Consulting
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SUMMARY

Electrical Engineering Consultant with 45 years of experience in integrated circuit simulation and design. Developed the SPICE circuit simulation program at UC Berkeley and the ADVICE circuit simulation program at Bell Laboratories. Technical strengths include analog circuit design, circuit simulation, semiconductor device modeling, and integrated circuit processing technology. Other strengths include project management, communication, and leadership skills emphasizing team building.

EDUCATION

PhD, EECS, 1975, University of California, Berkeley, CA
Research Advisor: Donald O. Pederson.
Thesis title: *SPICE2: A Computer Program to Simulate Semiconductor Circuits*.

MS, EECS, 1971, University of California, Berkeley, CA
Research Advisor: Ronald A. Rohrer.
Report title: *Computer Analysis of Nonlinear Circuits, Excluding Radiation (CANCER)*

BS, EECS, 1969, University of California, Berkeley, CA
Graduated with honors.

EXPERIENCE

2008 – present **Omega Enterprises Consulting,** Kensington, CA
President

Relocated Omega Enterprises to California to continue to provide consulting services in the areas of analog and RF circuit simulation, semiconductor device modeling, and analog and RF integrated circuit design, providing assistance in the assertion and interpretation of patents and trade secrets involving semiconductor devices and circuit design techniques, and serving as an expert witness in patent and trade secret litigation. Client list is available upon request.

2015 – 2015 **Chabot College,** Hayward, CA
Adjunct Professor

Taught two engineering courses in the Spring Semester, 2015 at Chabot College, a community college, while the engineering professor was on sabbatical. Taught the freshman course ENGR10, Introduction to Engineering, and the sophomore course ENGR43, Engineering Circuit Analysis.

1998 – 2008 **Omega Enterprises,** Randolph, NJ
Proprietor

Founded Omega Enterprises to provide consulting services in the areas of analog and RF circuit simulation, semiconductor device modeling, and analog and RF integrated circuit design, providing assistance in the assertion and interpretation of patents and trade secrets involving semiconductor devices and circuit design techniques, and serving as an expert witness in patent and trade secret litigation. Client list is available upon request.

1996 – 1998 **Anadigics, Inc.** Warren, NJ
Director, Technology Development

Responsible for device characterization, device modeling, and circuit simulation efforts for both internal GaAs MESFET processes and external foundry GaAs MESFET processes, silicon CMOS processes, and exploratory processes.

- Managed a team of 10 engineers to provide device characterization, device modeling, and circuit simulation capabilities for all Anadigics technologies.
- Participated in a team effort to import a suite of CMOS design tools to develop a frequency synthesizer that was operational on the first turn.

1995 – 1996 **Anadigics, Inc.** Warren, NJ
Manager, Circuit Simulation

Responsible for device characterization, device modeling, and circuit simulation efforts for Anadigics GaAs MESFET processes.

- Managed a team of 4 engineers to support device characterization, device modeling, and circuit simulation for Anadigics GaAs MESFET processes.
- Participated in a team effort to identify and characterize device anomalies observed in Anadigics GaAs MESFET processes.

1991 – 1995 **AT&T Microelectronics**, Allentown, PA
Technical Manager, TCAD Product Development Group

Managed the deployment of Technology CAD Tools to AT&T customers and support of two and three-dimensional interconnect simulation tools.

- Managed a team of 10 software engineers to develop alpha and beta versions of the Celerity analog simulation tool.
- Participated in a team effort to implement a quality system for the department in the successful effort to achieve ISO 9001 certification.

1989 – 1991 **AT&T Intellectual Property Division,** Liberty Corner, NJ
Intellectual Property Manager

Reviewed the technical merits of AT&T patents. Performed financial analyses of competitors. Responsible for reverse engineering of competitors' products to establish possible use of AT&T patents. Member of a team to negotiate patent licenses.

- Negotiations with two major semiconductor companies.
- Negotiated equipment contracts with Nippon Telephone & Telegraph.

1984 – 1989 **AT&T Bell Laboratories**, Murray Hill, NJ
Supervisor, High Speed Analog IC Group

Managed the design of prototype analog circuits, high frequency device modeling, final process testing, and computer aided design support. Supervised eight engineers.

- Designed high-speed analog circuits for submicron technologies.
- Supported work in noise measurements and s-parameter characterization.
- Assisted the Final In-Process Testing effort.

1979 – 1984 **Bell Laboratories**, Murray Hill, NJ
Supervisor, Device Characterization and Simulation Aids Group

Managed development of circuit simulation, device modeling, and technology characterization.

- Provided support for the ADVICE circuit simulation program.
- Supported development of the BICEPS process simulation program.
- Participated in the development of a compact model for bipolar transistors that included quasi-saturation effects in the Gummel-Poon bipolar model; this model later would become known and the Kull-Nagel model.

1974 – 1979 **Bell Laboratories,** Murray Hill, NJ
Member of Technical Staff, Device Characterization and Simulation Aids Group

Developed circuit simulation tools.

- Developed the ADVICE circuit simulation program.
- Participated in the development of the CSIM compact model for MOSFETs.
- Assisted circuit designers in applying ADVICE to the design of analog circuits, dynamic memories, and microprocessors.

IEEE PROFESSIONAL ACTIVITIES

IEEE Outstanding Engineer Award, Central Area, Region 6 (2016)

IEEE Outstanding Engineer Award, Santa Clara Valley Section (2016)

IEEE Life Fellow (2012 – present)

IEEE Fellow (2005 – 2011)

IEEE Senior Member (2003 – 2004)

IEEE Member (1975 – 2002)

IEEE Behavioral Modeling and Simulation (BMAS) Workshop (2007 – 2010)

- Member of Technical Committee (2007 – 2010)
- Technical Program Chair (2007)
- General Conference Chair (2008, 2010)

IEEE Bipolar Circuits and Technology Meeting (2001 – 2007)

- Member of Technical Program Committee (2001– 2007)
- Chair, Modeling and CAD Subcommittee (2006 – 2007)

IEEE Consultants' Network of Northern New Jersey (1998 – 2008)

- Secretary (1999-2001)

IEEE Consultants' Network of Silicon Valley (2009 – present)

- Chair (2010 – 2011)
- Director (2012 – present)

IEEE Custom Integrated Circuits Conference (2001 – present)

- Member of Technical Program Committee (2001 – present)
- Chair, Modeling and Simulation Subcommittee (2002 – 2005)
- Co-chair, Education Sessions Committee (2005)
- Chair, Education Sessions Committee (2006 – 2007)

IEEE Electron Device Society Distinguished Speaker (2006 – 2008)